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│        CIRCUITS RUMP SESSIONS        │
│          Thursday, June 17           │
│        8:00 p.m. – 10:00 p.m.        │
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Organizers: S. Kosonocky, IBM
                     M. Nagata, Kobe University

R1:   Limitations of Low FO4 Designs
Honolulu I
Organizers/Moderators: S. Butler, AMD
                         F. Arakawa, Hitachi

The session will discuss the tradeoffs between enabling higher clock frequencies by reducing the number of logic gate delays, measured in fan-out of 4 (FO4) inverters in each pipe stage versus the overhead and inefficiencies of deeper pipelines. Trade-offs balancing performance, power, area, time to market, electrical analysis and marketing of higher clock frequencies will be debated. Given the acceptance of the personal computer as a standard consumer appliance and therefore the importance of consumer marketing, and the rapid transition from desktop computing to battery-conscious mobile platforms, the continued penetration of embedded computing, handheld devices, and the extremely competitive nature of the microprocessor business, there will be many interesting points of agreement and disagreement.

Panelists:
H. Ando, Fujitsu   N. Nishi, NEC
C. Johnson, IBM   O. Nishii, Super H
R. Kumar, Intel   W. Walker, AMD

R2:   The Future of Embedded SRAM – Cornerstone or Millstone?
Honolulu II
Organizers: S. Natarajan, MoSys
                     K. Ishibashi, STARC
Moderators: B. Bateman, T-RAM

The six transistor (6T) SRAM has been used as on-chip RAM on systems LSIs because of its high speed and low characteristics. Low voltage functional operation of the device is another critical factor in addition to area, speed, power and hence 6T SRAMs may not continue to serve the same trend of benefits for future technology generations. The 6T SRAM has issues of (1) low voltage operation due to large leakage by low threshold voltages (2) electrical stability degradation caused by ever-larger mismatches between paired MOSFETs in future advanced technologies and (3) SER sensitivity degradation. Embedded 6T SRAMs are perfectly compatible with current SoCs demands com-pared to other memory technologies, without additional process cost and the added benefit of compilability. The panel will address the feasibility of SRAMs for on-chip embedded memory for future technologies and con-clude if the newer proposals of on-chip memory technologies such as FRAM, MRAM, or Ovonic memories can compete with SRAMs in the future. Will 6T SRAMs last forever or fade away? Are there design solutions that can resolve all of these above issues and allow 6T SRAM to continue as the mainstream embedded memory? How premature are the newer memory technologies and in what capacity can they compete with 6T SRAMs? Will new memory technologies be SoC compatible, if so at what cost?

Panelists:
K. Itoh, Hitachi   H. Pilo, IBM
H.G. Byun, Samsung   P. Rickert, Texas Instruments
S. Masui, Fujitsu   A. Shubat, Virage Logic

R3:   Analog CAD: Computer Aided Design or Computer Accelerated Disasters?
Honolulu III
Organizers/Moderators: P. Kinget, Columbia University
                         A. Matsuzawa, Tokyo Inst. of Tech.

Analog and RF interfaces are very critical parts in current 'System on a Chip' (SoC) designs. The number of transistors in the interfaces is relatively small but they take a long time to design and often require design re-spins. As a result, design productivity appears poor. The success of a project critically depends on highly experienced circuit designers and they remain a scarce resource. For several decades, there has been an ongoing quest for CAD tools and automated design technologies for analog and RF. Recently several new tools have been brought to the market. This panel will discuss field-tested analog CAD tools and automated analog design technologies. How do they help to shorten time to market? Do they enable a faster migration to small feature size technologies and analog IP block reuse? Or do they replace sound, time proven design techniques with methodologies that (over) rely on CAD technology with disastrous consequences

Panelists:
P. Daglio, STMicroelectronics   T. Miki, Renesas Technology
S. Doushoh, Matsushita Electric   M. Ugajin, NTT
D. Mercer, Analog Devices